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Heterogeneous 3-D circuits: Integrating free-space optics with CMOS

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ABSTRACT

A three-dimensional (3-D) integrated circuit combining free-space optical interconnects (FSOI) with CMOS devices has been developed. An overview of the combined optical and CMOS system is described. Experimental data and simulated results are provided. A 3-D integrated test circuit merging the free-space optical network with gallium arsenide based vertical cavity surface emitting lasers (VCSELs) and germanium based photodetectors has been experimentally tested. The prototype 3-D IC test circuit exhibits a 3.3 GHz bandwidth and a 5.1 mW total power consumption per link. The bandwidth is limited due to the use of 5 GHz bandwidth commercial VCSELs and the large inductive impedance of the wirebonds attaching the VCSELs and photodetectors to the I/O pads. The design of transmitter circuits for the 3-D integrated free-space optical interconnect system is discussed, and simulated extrapolated results on operating frequency and bandwidth are provided. The microprocessor operates at 333 MHz and includes a bus width of 64 bits, requiring a FSOI bandwidth of 10.65 Gbps after serialization.

1. Introduction

One substantial benefit of 3-D integration is the potential to integrate a variety of technologies without compromising yield. Disparate technologies such as analog, III–V semiconductors, RF, memory, and optics, as well as emerging technologies such as nanowire and graphene can be integrated to form a 3-D system. Separate processing of each device plane prior to bonding and TSV formation allows for wafer and die level testing to ensure proper functionality of the devices. Merging disparate technologies with CMOS, however, often requires different currents, synchronization methodologies, and voltages among the device planes. Systems level integration with CMOS is therefore an on-going research objective [1–4].

A technology that can potentially lead to improved circuit performance, reduced power consumption, and increased functionality is on-chip optical interconnects. Integrating optical interconnects with traditional CMOS technology can reduce delay and increase bandwidth as compared to metal interconnects [5–7]. Integrating photonic devices with silicon has progressed significantly in recent years [8,9]. Much of this work however, has focused on optical interconnect using planar optical waveguides, which are integrated onto the same die as the CMOS devices. A limitation of optical waveguide interconnects is the current lack of optical switches and storage devices. Without these switches and storage devices, routing and flow control in a packet-switched network requires repeated optoelectronic (O/E) and electro-optic (E/O) conversions, which significantly increases signal delay, energy consumption, and circuit complexity. In addition, efficient silicon electro-optic modulators are a challenge to manufacture due to the inherently poor optical properties of silicon and other weaker physical properties such as the plasma dispersion effect [10]. The modulators, therefore, require a long optical length, resulting in large device sizes [11]. Techniques to reduce the size of the modulator devices, such as high-Q resonators (ring, microcavity, or micro-disk), effectively slow the light [12] at a cost of increased delay and reduced bandwidth.

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An additional drawback of in-plane waveguides is the mode diameter, which determines the minimum distance between optical waveguides to avoid crosstalk. Existing distances are significantly greater than the electrical interconnect pitch at sub-micrometer technology nodes and is expected to become smaller as CMOS technologies scale [13]. Although wavelength division multiplexing (WDM) has proven effective in long distance fiber-optic communication systems, it is not practical for intra-chip optical interconnects due to the significant power and area overhead required for wavelength multiplexers and demultiplexers, and the requirement for multiple external laser sources operating at different wavelengths.

One solution is a heterogeneous 3-D system that includes an optical device plane integrated with a CMOS plane. The optical device plane operates as a free-space interconnect system, thereby eliminating the switches and storage devices required with optical waveguides. Free-space optics has been applied to both board-to-board [14,15] and inter-chip communications [16,17]. The added benefit of a 3-D IC hybrid system is that the optical devices can be fabricated on materials traditionally used for optics such as GaAs and SiGe, removing the need for the optics to be integrated in silicon. The lasers, modulators, and photodetectors are available in III–V semiconductors and can be assembled with a CMOS SoC using 3-D integration technology.

These technologies include emerging devices and CMOS circuits. The optical devices are leveraged to provide an interconnect architecture without network router nodes. The primary technologies required to develop a free-space optical interconnect (FSOI) are:

- *Signaling*: Vertical cavity surface emitting lasers (VCSEL) provide light emission without the need for external laser sources and to route the optical power supply throughout the IC. VCSELs, photodetectors (PDs), and the supporting micro-optic components are developed in GaAs, Ge, or silica technologies and integrated into a 3-D silicon system, which includes CMOS digital electronics as well as the transmitters and receivers for the optical communication network.
- *Propagation medium*: Free-space optics using integrated micro-optic components provide high speed signal propagation with low loss and low dispersion.
- *Networking*: Direct communication links through dedicated VCSELs, PDs, and micro-mirrors (in small-scale systems) or via phase array beam-steering (in large-scale systems) allow a quasi-crossbar structure that avoids packet switching, offer ultra-low communication latency, and provide scalable bandwidth due to the fully distributed nature of the optical interconnect.

The primary goal of the research project is not to target any one particular type of signal, but rather to validate the concept of integrating free-space optics with CMOS as a low power, high bandwidth system level communication fabric. Work describing the optical components of the free-space optical interconnect have been published by this group. A description of photodetectors designed and fabricated by the group is provided in [18]. The prototype of the free-space optical system summarized in this paper is discussed in [19]. In addition, a study on the architectural benefits of an integrated SoC including free-space optics with CMOS for an ultra-low transmission latency and highly scalable bandwidth system has been described in [20]. This paper provides a discussion of the system level integration of the optical devices and electrical components. In addition, the CMOS electrical device planes are discussed for the first time, including the transceiver and microprocessor.

The 3-D integrated free-space optical interconnect system is described in Section 2. A description of the optical device plane is provided in Section 3. The transceiver circuits, necessary for the electrical and the optical communication network and the microprocessor core to verify core-to-core transmission, are described in Section 4. Some concluding remarks are provided in Section 6.

2. Overview of 3-D integrated FSOI

An overview of the intra-chip optical interconnect system for multi-core processors incorporating free-space optics with the 3-D integrated photonic and CMOS devices is provided in this section. The objective is to provide point-to-point links constructing an all-to-all communication network with high bandwidth density, low latency, and high energy efficiency without the need for routing or switching optical data packets. The 3-D integrated free-space optical interconnect (FSOI) system is illustrated in Fig. 1. Three distinct layers of devices are integrated to produce a 3-D integrated FSOI. The three components comprise (1) a CMOS device plane consisting of the transceiver and microprocessor circuits, (2) a photonics layer consisting of vertical-cavity surface emitting lasers (VCSEL) and photodetectors (PD), and (3) a free-space optical guiding medium constructed from micromirrors and microlenses.

The free-space optics enables an N-to-N direct communication structure, where each core within a multi-chip module (MCM) contains a dedicated VCSEL and PD. The optical signal generated by an electrically modulated VCSEL in one core is focused by a microlens on the backside of the GaAs substrate. Electrical modulation is performed by transmitter circuits in the CMOS device plane that provide a signal to the VCSELs through the substrate with through silicon vias. The optical signal is guided across the IC by mirrors located on the IC and package (the top device layer shown in Fig. 1). Once the signal propagates to the target core, a microlens focuses the signal onto a photodetector, where the optical signal is converted back into an electrical signal. The electrical signal is filtered and amplified by the receiver circuitry at the destination core. Note that, unlike waveguides, the electrical-to-optical and optical-to-electrical conversion only occurs once from the originating core to the destination core, reducing both delay and power consumption.

The free-space optical interconnect exhibits several distinct advantages over other optical interconnect techniques. These advantages include:

- Low latency, as no packets are switched (therefore the associated intermediate routing, buffering, and arbitration delays are avoided).
- Low propagation loss, minimal dispersion, and low bandwidth degradation with transmission distance.
- Good signal integrity simplifies the CMOS transceiver electronics (a single laser driver in the transmitter and a single amplifier in the receiver).
- Reduced power consumption by eliminating packet-switching, powering down the VCSELs during low duty cycle operations, and avoiding thermal tuning of sensitive electro-optical modulators in WDM systems.
- Easily adjusted to included inter-chip communication pathways (as shown in Fig. 1(a)).

A description of each of the optical components comprising the optical device planes is provided in the following section.

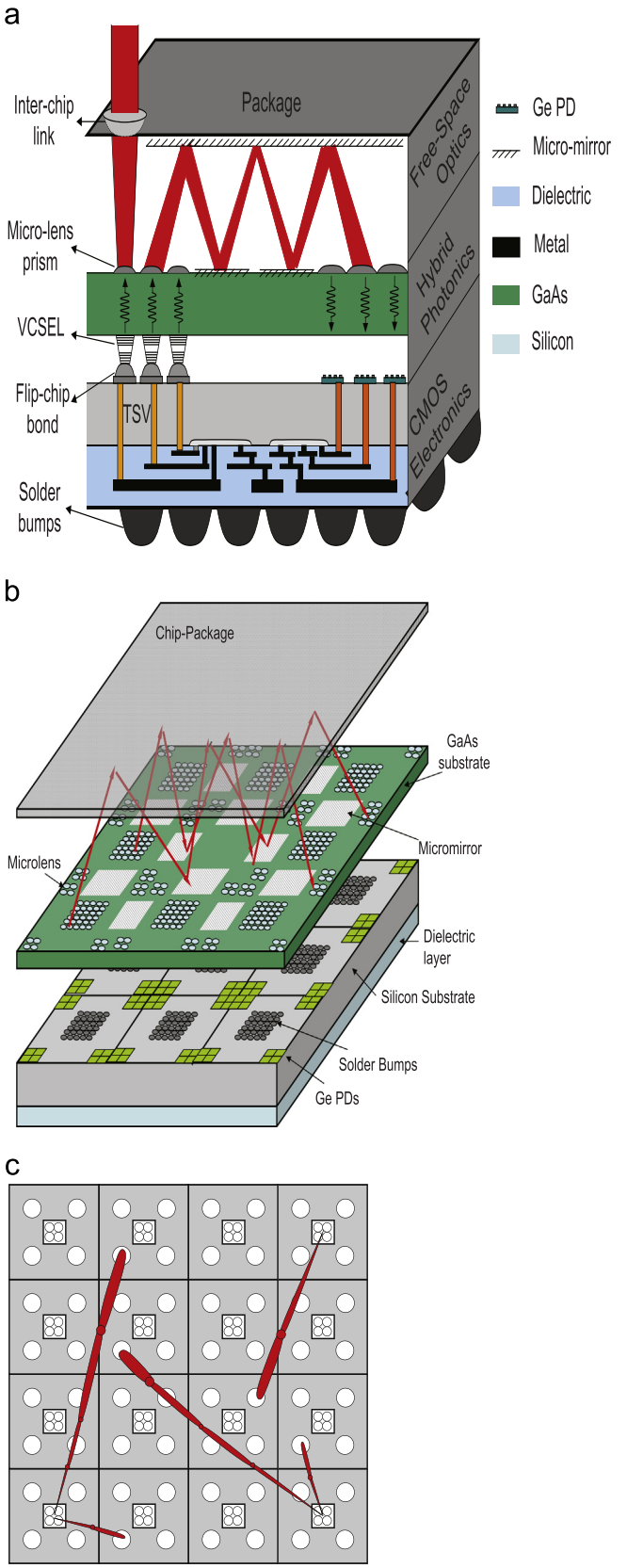

Fig. 1. Schematic representation of the 3-D integrated FSOI including (a) a cross-sectional view of the FSOI with the intra- and inter-core communication links, (b) the FSOI system with VCSEL arrays (center) and photodetectors (periphery) to signal a multi-core microprocessor, and (c) a top view of the core-to-core optical transmission [19–21].

3. Components of the optical system

The primary optical components of the 3-D integrated free-space optical interconnect system are the vertical cavity surface emitting lasers (VCSEL), the photodetectors (PD), and the micro-mirrors/microlenses. The optical components are designed to operate at a wavelength of 850 nm. Each of these components of the 3-D integrated FSOI system was fabricated at the University of Rochester. The three components are described below.

3.1. Vertical cavity surface emitting laser (VCSEL)

The vertical cavity surface emitting laser is a fundamental technology that integrates the optical communication network with the CMOS device planes. The VCSEL converts electrical signals into light which is transmitted through the free-space optical system to the destination core. The VCSELs described in this sub-section operate at a 980 nm wavelength, whereas the remaining components are designed to operate at 850 nm to match the commercial VCSELs used in the prototype circuit. Once in-house VCSELs are produced, the commercial VCSELs will be replaced and the PDs and other optical components will be adjusted to 980 nm.

The VCSEL includes an intra-cavity contact, an oxide aperture, and AlAs/GaAs distributed Bragg reflectors (DBR) mirrors. A schematic view of the VCSEL structure is shown in Fig. 2, which also includes the substrate. The intra-cavity resonator is an arrangement of mirrors (AlAs/GaAs DBR) forming a standing wave cavity resonator by surrounding the gain medium that amplifies the light wave. Bragg reflectors consist of an alternating sequence of high and low refractive index layers with a quarter wavelength thickness [22]. In addition, AlAs/GaAs DBRs have been shown to form uniform and smooth heterointerfaces, yielding mirrors with high reflectivity [22,23]. The thick top DBR and bottom DBR outline the active region of the device. More than 20 Bragg pairs are typically required for each mirror [22]. The intra-cavity contact improves the speed characteristics of the VCSEL. The two metal square loops connect above and below the active region of the quantum well through the heavily doped ($p++$ and $n++$) GaAs contact layers. The doping concentration of the $p++$ and $n++$ contact layers are, respectively, $5\times10^{18}\ cm^{-3}$ and $3\times10^{18}\ cm^{-3}$. Each contact layer is 208.6 nm thick and is located between the DBR mirrors and AlAs layers. This structure has both electrical and optical advantages. The vertical current injection path is reduced by as much as 90% without passing through the thick layer of the AlAs/GaAs mirrors. The two 83.8 nm AlAs lateral oxide layers shape the optical aperture and encapsulate the active region to reduce the threshold current while improving the quantum efficiency of the VCSEL. The active region is composed of three 8 nm $In_{0.2}Ga_{0.8}As$ quantum wells (QWs) and four 10 nm GaAs barrier layers, and is covered by two 116.8 nm thick $Al_{0.5}Ga_{0.5}As$ spacer layers. The total thickness of the core, approximately 300 nm, is about one-third of a wavelength. In addition, since no current flows through the DBR mirrors during laser operation, the mirrors are undoped, which minimizes optical absorption and carrier scattering inside the mirror region. Note that the total thickness of the active region, aperture layers, and contact layers is one wavelength, about 980 nm [19,21,24].

A top view of the VCSEL is shown in Fig. 2(b). The VCSEL is typically designed with a circular or square aperture. In this case, anisotropic oxidization of AlAs produces a non-circular aperture despite a circular active region mesa [25]. A square mesa is therefore fabricated rather than aligned with the sides along the $<100>$ crystal lattice axes, which exhibits a higher oxidation

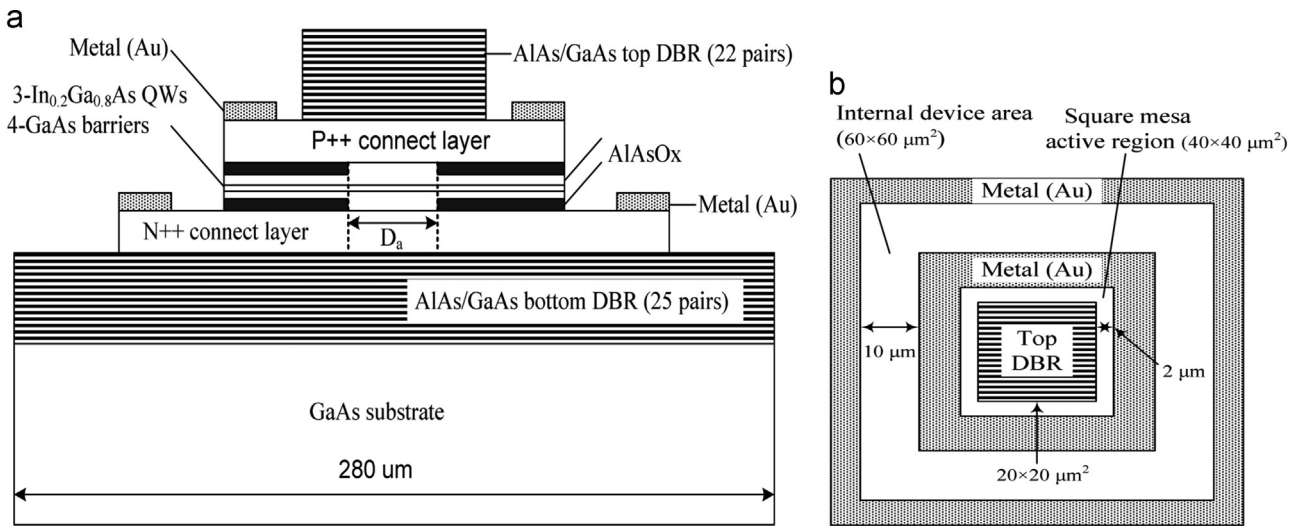

Fig. 2. Schematic diagram of VCSEL structure (a) side view, and (b) top view.

rate than the $<110>$ direction. The top mirror, active region (square mesa), and internal device area (without the N++ metal contact) are, respectively, $20\times20\ \mu m^2$, $40\times40\ \mu m^2$, and $60\times60\ \mu m^2$. The minimum pitch size for the VCSEL array is equivalent to three times the width of the active area, and is 120 μm. Also shown in Fig. 2(b) is the 2 μm space between the metal to the P++ contact and the top mirror sidewall to avoid metal contamination of the top mirror, and the 10 μm space between the metal contacts to facilitate the lift-off process. The lift-off process releases the substrate from the VCSEL structure that includes the epitaxial DBRs [26].

3.2. Photodetectors

The photodetectors receive optical signals at the receiver of the destination core. Light is absorbed and converted to an electrical signal by the PD. The photodetectors are designed to support a 7.5 Gbps data rate per link at 850 nm. The semiconductor material used to produce the PDs is germanium. Germanium based PDs are easier to integrate with CMOS, and exhibit strong optical and electrical properties that increase sensitivity and bandwidth [18]. A metal–semiconductor–metal (MSM) structure is chosen over a p–i–n structure to reduce the parasitic capacitance per unit area. With a reduced parasitic capacitance, the strict alignment requirements of the microlens with the PDs to efficiently couple the light can be loosened without degrading the bandwidth or responsivity [18,19].

The physical and electrical properties of the germanium MSM PD have been characterized after fabrication. Each PD is 62 by 62 μm^2 with a parasitic capacitance of 83 fF. The PD also exhibit a 0.315 A/W responsivity and a 7 μA dark current. The experimentally measured dark current is larger than simulated results. The higher experimental value is primarily due to accidental plasma damage at the hydrogenated amorphous silicon (a-Si:H) layer during etching of the Si_3N_4 layer, increasing surface trap states at the a-Si/Si_3N_4 interface [19]. The photodetector bandwidth is 9.45 GHz at a 7 V bias and 10.05 GHz at a 10 V bias, as shown in Fig. 3. The bandwidth is primarily limited by the transit time of the carriers and the impedance of the wirebonds from the IC to the circuit board.

Additional details on the photodetectors are provided in [18,19]. The photodetectors are but one component of the heterogeneous CMOS and free-space optical system described in this paper. A system level description of the overall SoC is described

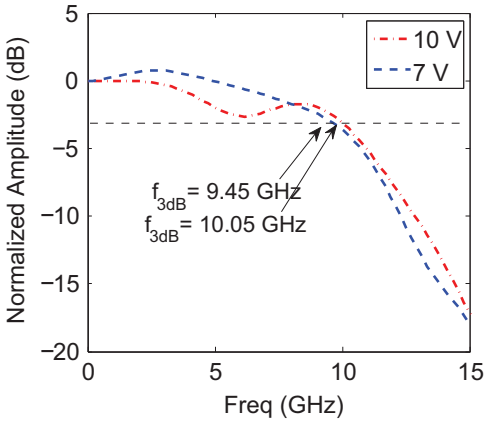

Fig. 3. Converted measurement results using Density Functional Theory (DFT) for the 62 by 62 μm^2 area Ge MSM photodetector with 98-nm Si_3N_4 anti-reflection coating. The dark current density is measured as 1.7 nA/μm^2 at 7 volts [19].

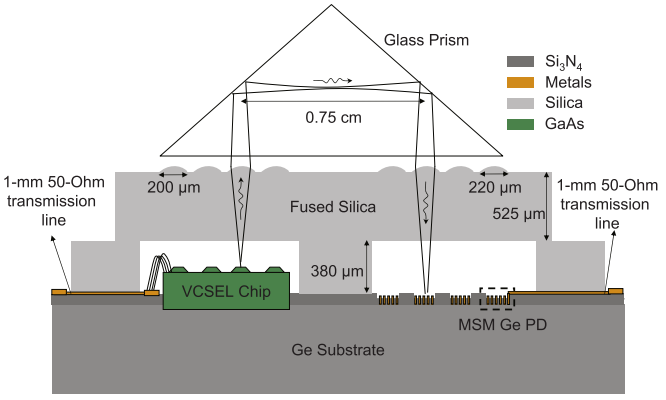

Fig. 4. Schematic of the test circuit that experimentally verifies the optical components of the 3-D integrated free-space optical interconnect system [19].

here whereas [19] provides greater detail describing integrating the optical components.

3.3. Micromirrors and microlenses

Microlenses and micromirrors are used twice within a single link of the FSOI system, as shown in Fig. 4. Microlenses are located directly above the VCSELs to focus the output light signal onto the

micromirror directly above which reflects the data signal through the free-space optical interconnect system. A second micromirror reflects the signal back towards a photodetector on a second core. The reflected signal passes through a second microlens that again focuses the lightwave onto the photodetector to lower optical loss.

The microlenses are made from fused silica. Fused silica offers a number of advantages including low optical transmission loss at 850 nm wavelength, is easily integrated with silicon substrates, and is compatible with CMOS processes [19]. The lenses are built by melting and reflowing photoresist into a spherical shape and dry etching the pattern into a 525 μm thick silica wafer. The thickness of the lens is 15.3 μm. The lens to lens pitch is 250 μm, matching the pitch of the VCSEL array. The fabricated microlenses for the VCSELs have a 200 μm aperture size with a corresponding focal point in air of 580 μm. Microlenses for the photodetectors have a 220 μm aperture and a 730 μm focal point (in air). All lenses exhibit a 1 dB optical scattering transmission loss. The total fused silica IC area is 0.84 by 0.84 cm^2 [19,21,27].

The micromirrors are fabricated directly on silicon or polymer substrates by micromolding techniques [28]. Greater than 99% reflectivity is achieved as the light reflects off the mirrors.

3.4. FSOI prototype test circuit

A prototype circuit has been tested to evaluate the optical device planes that includes the VCSELs, microlenses, and photodetectors. The micromirrors are replaced by a glass prism to simplify the testing process. In addition, commercial VCSELs are used for the prototype as the VCSELs produced by members of the University of Rochester team are not yet available. The commercial VCSELs are Finisar V850-2092-001S, sold as a 1 by 4 array with a pitch of 250 μm. Each VCSEL provides a 2 mW optical power output at 850 nm with a 5 GHz modulation bandwidth. The commercial VCSELs also have an aperture size of 8 μm and a full width half-maximum far-field divergence angle of 20° in free-space at the operating bias point.

The prototype includes the 3-D integration of the VCSELs, microlenses, and photodetectors, as shown in Fig. 4. The photodetectors have been fabricated on a germanium (Ge) substrate. The VCSELs are integrated with the PDs on the germanium carrier with high horizontal accuracy and minimal tilt and rotational error [19]. A non-conductive epoxy is used to bond the commercial VCSELs to the Ge carrier, and wirebonding is used to electrically connect the devices. The alignment tolerance is limited to a few micrometers due to the 0.5 μm optical stage resolution and a maximum ±5 μm axial placement uncertainty of the VCSELs. After bonding, the VCSELs and PDs are 0.75 cm apart. In addition, the VCSELs are wirebonded to 1 mm long 50 Ω transmission lines on the Ge substrate. Each PD is also bonded to a 1 mm long feed line for testing.

The VCSELs and PDs are integrated onto the Ge carrier with the microlenses and micromirrors. A 380 μm spacer layer of silica is bonded to the Ge carrier to ensure the vertical space between the bondwires for the VCSELs and PDs located between the carrier and microlens. The fused silica microlens die is aligned to the Ge carrier and glued with a non-conductive epoxy. The measured tilt of the microlens die after integration is less than 4 μm from one edge to the other edge [19]. As there is an approximately 200 μm difference in height between the VCSELs and PDs (as shown in Fig. 4), the microlens aperture and focal length have been adjusted to match the required conditions of each device. As previously mentioned, the microlenses have a 200 μm aperture size and 580 μm focal point for the VCSELs, and a 220 μm aperture size and 730 μm focal point for the PDs.

Experimental results from the prototype indicate a 3 dB bandwidth for the FSOI link of 3.3 GHz (as shown in Fig. 5) with a total power consumption of 5.1 mW. The electrical-to-electrical current gain of the optical link is measured as −24.4 dB at a 1 cm distance and −26.6 dB at 1.4 cm (total path distance from VCSEL to the PD). The crosstalk between adjacent links is −23 dB for a path length of 1 cm and −16 dB for a 2 cm long path [19]. Additional characteristics of the integrated optical system are provided in [19].

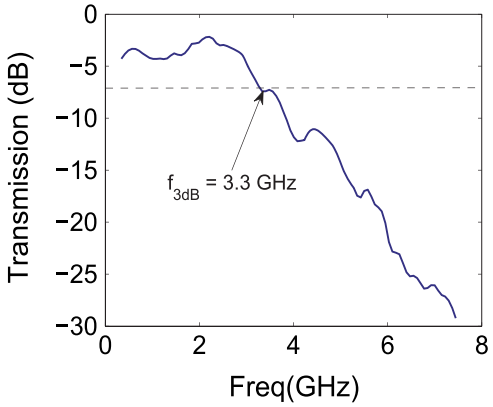

Fig. 5. Small-signal bandwidth at a distance of 1 cm. Note that the optical transmission changes between −4 and −5 db at 1 cm distance due to the reflection and scattering losses of the lenses. The sharp increase in loss due to distance can be alleviated by using larger numerical aperture (NA) lenses [19].

4. 3-D integrated CMOS transceiver and microprocessor circuitry

In addition to the optical components of the 3-D integrated free-space optical interconnect system, a transceiver and microprocessor are also included to provide, respectively, signal control (electric-to-optic and optic-to-electric conversion, amplification, and filtering) and generation of the electrical data for transmission over the FSOI. Both the transceiver and microprocessor are currently in fabrication (Tezzaron Semiconductor). Tezzaron provides two logic device planes integrated within a 3-D system with 1.2 μm diameter TSVs to form a stacked die. Each logic device plane is separately processed by Chartered Semiconductor (currently a subsidiary of GlobalFoundries) in a 130 nm CMOS process technology prior to 3-D bonding, TSV fabrication, and wafer thinning, which is completed by Tezzaron.

The Chartered fabrication process includes low power 1.5 V and 2.5 V transistors, six metal layers per device plane, a single polysilicon layer, dual gates for the 2.5 V transistors, and low and nominal threshold devices [29,30]. The sixth metal level on each die is allocated for face-to-face bonding to vertically stack the two logic device planes. A microphotograph of the fabricated 3-D integrated logic planes is shown in Fig. 6(a). The location of the transmitter and receiver circuits on the top logic die, and the microprocessor on the bottom logic die are shown, respectively, in Fig. 6(b) and (c). A description of the FSOI tranceiver is provided in the following subsection, while an overview of the microprocessor is provided in Section 4.2.

4.1. FSOI transceiver circuitry

The transceiver circuitry is composed of isolated transmitter and receiver circuits. The transmitter converts an electrical signal from a logic core to an optical signal for transmission by the free-space optical network. Receiver circuits convert the optical signal to an electrical signal at a destination core. A schematic of the transmitter, FSOI, and receiver circuits is shown in Fig. 7. A shared-

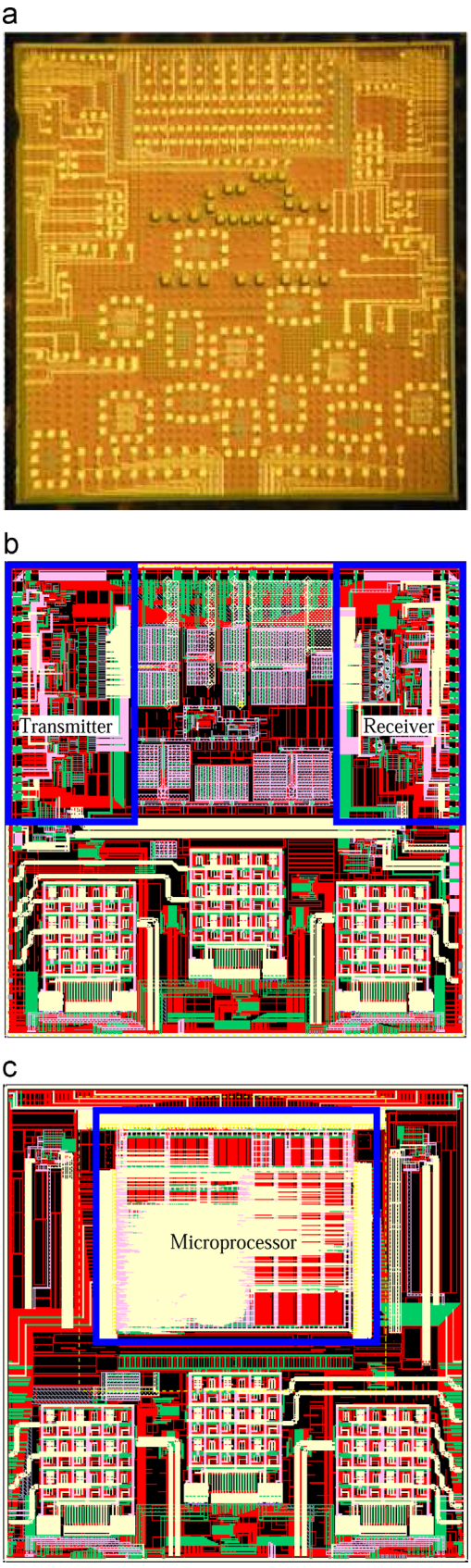

Fig. 6. (a) Microphotograph of the fabricated 3-D integrated logic dies, (b) layout of the top logic die, and (c) layout of the bottom logic die. The two individual CMOS logic dies are bonded to form a 3-D IC.

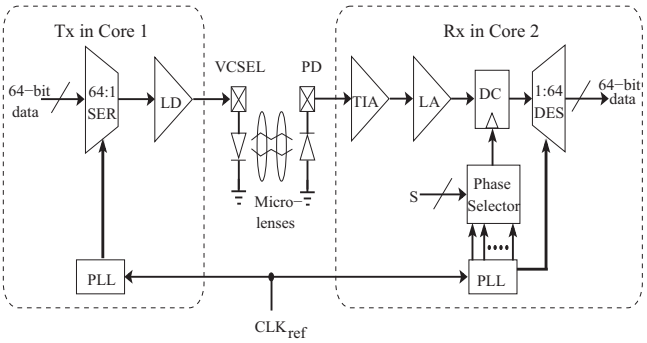

Fig. 7. Schematic representation of the transceiver circuitry included in the CMOS device plane [33].

clock transceiver simultaneously shares the reference clock between the transmitter and the receiver [31,32]. A shared-clock architecture is well suited for systems with multiple transceivers, such as multi-channel or multi-core systems, as a global clock distribution network is typically available to provide synchronization to each channel or core with no additional hardware. The clock signal is distributed among the different cores through a global distribution network. A brief description of both the transmitter and receiver circuits follows.

The transmitter consists of three components: a serializer (SER), laser driver (LD), and phase locked loop (PLL). The SER serializes the n-bit low speed parallel outputs from the microprocessor core and feeds the high speed serialized output to the laser driver. In the FSOI system, a 64 bit to 1 bit SER produces one high speed 10 Gb/s data signal. The PLL provides the reference clock frequency (10 GHz) for the SER. The SER is based on a binary tree architecture consisting of a set of 2-to-1 multiplexer circuits, where each stage shares one clock for control and synchronization. Based on the serialized data from the SER, the laser driver delivers the corresponding modulation current to the VCSEL, which converts the electrical signal to an optical signal transmitted by the FSOI [33]. The simulated and experimental results of the frequency dependent gain of the laser driver are shown in Fig. 8(a).

The receiver circuitry consists of six components: (1) transimpedance amplifier (TIA), (2) limiting amplifier (LA), (3) decision circuit (DC), (4) phase selector, (5) phase-locked loop (PLL), and (6) deserializer (DES). An optical signal is converted into an electrical signal by the photodetector. The TIA converts the output current from the photodetector into a voltage with sufficient gain and bandwidth. The output signal from the TIA is further amplified by the LA to satisfy the input sensitivity requirements of the data recovery circuit (the decision circuit). As substantial noise exists in the received data, a decision circuit is placed between the limiting amplifier and the deserializer to sample the amplified signal from the limiting amplifier and pass a low noise output to the deserializer. The phase selector generates the optimal phase to trigger the decision circuit sampling the data [33]. The PLL is identical to the circuit used in the transmitter, and can therefore be shared by the transmitter and receiver. A single PLL is therefore needed per core. In the receiver, the PLL is used for both the deserializer and multi-phase clocks in the decision circuitry. The DES converts the high speed 10 Gb/s serial data to 64 bit low speed parallel data passed to the microprocessor core. The simulated and experimental results of the gain as a function of frequency for the receiver front-end circuit with an active transimpedance amplifier (TIA) is shown in Fig. 8(b).

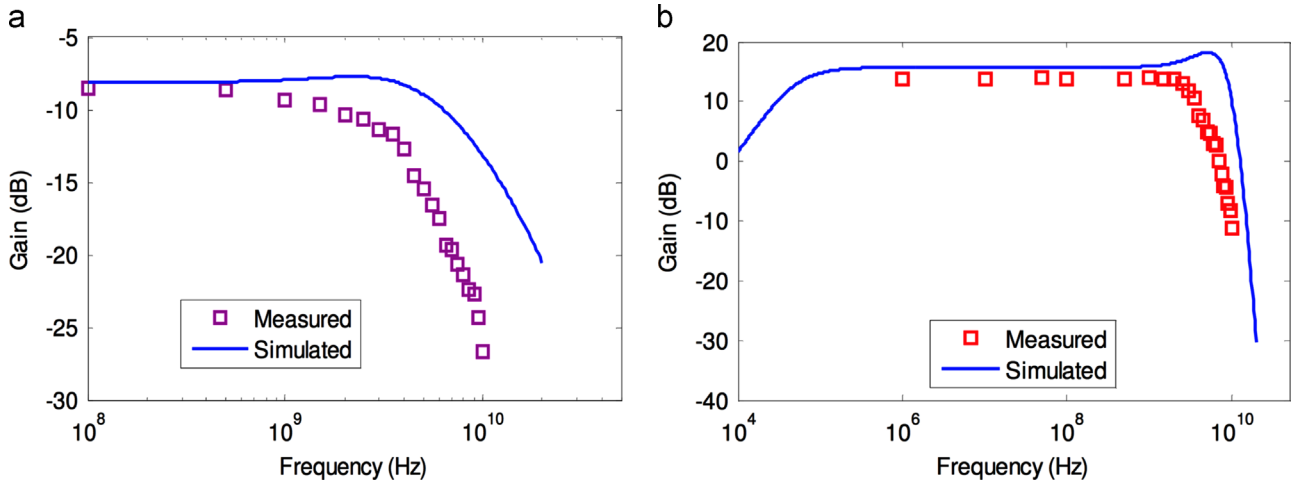

Fig. 8. Measured and simulated results characterizing the frequency dependent gain of the (a) laser driver of the transmitter circuit, and (b) receiver circuit with active transimpedance amplifier (TIA) [33].

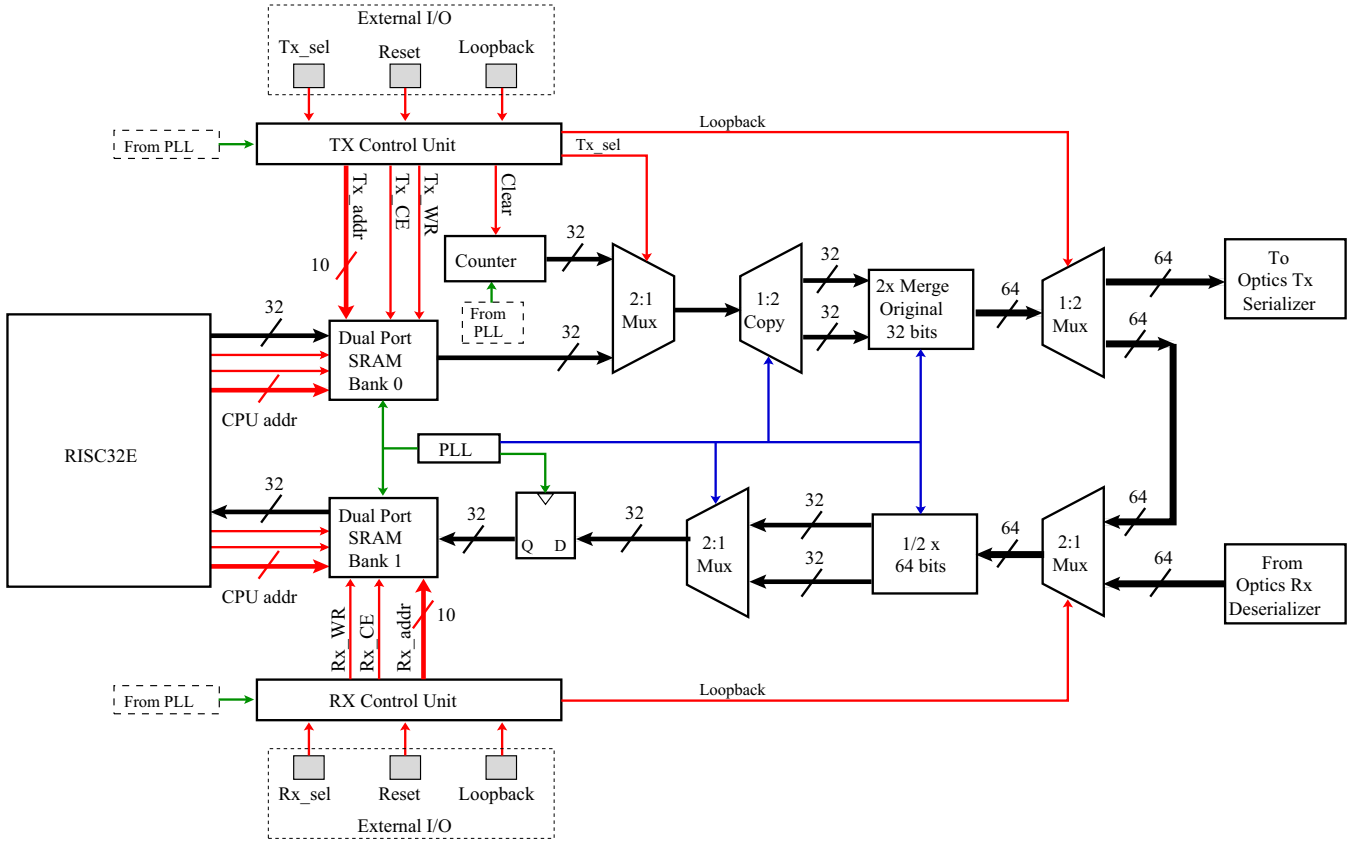

Fig. 9. Schematic block representation of the transmitter and receiver at the interface between the RISC32E and the 64 bit serializer and deserializer. The transmitter is on the top half of the figure, while the receiver is on the bottom half.

4.2. *Integrated microprocessor cores*

The microprocessor core generates and receives data from the FSOI through the transceiver circuits located on the top CMOS logic plane. The core is a high performance, low power 32 bit RISC (RISC32E) processor modified for custom system-on-silicon applications such as the 3-D integrated FSOI system [34]. The microprocessor core includes transmit and receive circuitry that interface, respectively, with the transmitter and receiver of the free-space optical interconnect. Both the microprocessor transmitter and the receiver are shown in Fig. 9. The transmitter includes two sets of data transmitted via the FSOI. The first data set is from the microprocessor core stored on a dual port SRAM (Bank 0 in Fig. 9). The SRAM is a 32 bit wide and 1 KWord long memory. The second data set, produced by a 32 bit counter, completely bypasses the microprocessor and generates data for diagnostics or if the core does not function properly. Since the serializer on the optical transmitter is 64 bits and both the microprocessor and counter produce 32 bit data, the 32 bit data set is copied by doubling the interconnect of the original 32 bit data set. This 64 bit data set is sent to the optical transmitter for serialization, as shown in the top half of Fig. 9.

The receiver performs similarly to the transmit circuit, but in the reverse direction. The optical receiver sends 64 bit deserialized

electrical data to the receiver within the microprocessor core, as shown in the bottom right corner of Fig. 9. The 64 bit data includes a copy of the original 32 bit data set, and either one of the two sets is discarded. The 32 bit data set is clocked into D flip flops, which is written into another dual port SRAM (Bank 1 in Fig. 9). The microprocessor reads the SRAM into local cache memory.

Control signals drive the transmitter and receiver circuits. Both the transmitter and receiver control units include write, clear, and 10 bit address lines. In addition, the transmitter control unit includes a clear line for the counter, and a transmitter select line that determines which data set is chosen for transmission (either the microprocessor or the counter data). Both the transmitter and the receiver control logic include a loopback line which verifies the functionality of the microprocessor transmitter and receiver by bypassing the free-space optical interconnect components. The loopback is a 64 bit bus that loops from the output of the 1:2 multiplexer in the transmitter to the input of the 2:1 multiplexer in the receiver, as shown on the right side of Fig. 9.

The microprocessor transmitter and receiver operate at one-half the core frequency. The core frequency is set to 333 MHz, mainly limited by the two dual port SRAM banks, and the transmitter and receiver therefore operate at 166 MHz. Since 64 bits are serialized and transmitted per optical link, an overall link bandwidth of approximately 10.65 Gbps is achieved.

5. System-level analysis

The proposed intra-chip free-space optical interconnect includes different design tradeoffs as compared with conventional wire-based interconnect or other optical systems. Some of these tradeoffs are not easily quantitatively characterized. System-level analysis of the proposed system indicates ultra-low latency, excellent scalability, and superior energy efficiency. In addition, tolerating collisions does not necessitate drastic bandwidth over-provisioning.

5.1. Simulation setup

An execution-driven simulator is used to model the system coherence, processor microarchitecture, communication network, and power consumption of a 16-way chip-multiprocessor (CMP) on SPLASH-2 benchmark applications. Details of the simulator are described in [20]. The effect of the FSOI system on latency, system performance, and energy consumption when the microprocessor is executing the SPLASH-2 benchmarks is analyzed below.

5.2. Performance analysis

The performance of the proposed integrated FSOI system is not the only figure of merit evaluated. Additional figures of merit are also considered as it is possible to make fast conventional electrical interconnect, but with highly complex routers and at a significant cost in energy.

The performance of the proposed interconnect is analyzed. A number of conventional interconnect configurations are modeled for comparison. A baseline system with canonical 4-cycle routers is used to normalize performance. Note that while the principles of conventional routers [35,36] and more recent circuits with shorter pipelines [37] are well understood, practical circuits require careful consideration of flow control, deadlock avoidance, order-of-service (QoS), and load-balancing. For example, the router in an Alpha 21364 has hundreds of packet buffers that occupy a physical area equal to 20% of the combined area of the core and 128 KB of L1 caches [38,39]. The router adds seven cycles of latency as data is transmitted.

A comparison with conventional interconnects with aggressive latency assumptions is performed. The average latency of transferring a packet in both free-space optical interconnect and in baseline mesh interconnect is shown in Fig. 10(a). The latency of the optical interconnect is affected by the queuing delay, intentional scheduling delay to minimize collision, actual network delay, and collision resolution delay. Despite the latency overhead of both the expected collisions and the techniques to prevent collisions, the overall delay of 7.5 cycles is low.

The speedup in execution time of the applications is shown in Fig. 10(b). The total execution time of the applications is used to compute the speedup, as compared to the baseline conventional mesh interconnect. As a relative comparison, a number of conventional configurations, such as L_0, L_{r1}, and L_{r2}, are modeled. For the L_0 case, the transmission latency is idealized to 0 and only the throughput is modeled. The only delay a packet experiences is the serialization delay (one cycle for meta packets and five cycles for data packets) and any queuing delay at the source node. L_0 is an idealized interconnect. Note that the L_O configuration is the best case scenario as the other electrical and optical interconnects cannot provide zero delay. L_{r1} and L_{r2} represent the cases where the overall latency accounts for the number of hops traveled: Each hop uses one cycle for link traversal and, respectively, one or two cycles for router processing. As with L_0, contentions or delays are not modeled inside the network, and only serve to illustrate loose performance upper bounds when aggressively designed routers are used [20].

While the performance gain varies between applications, a system that includes the free-space optical communication network accurately tracks the ideal L_0 configuration, achieving a 1.36

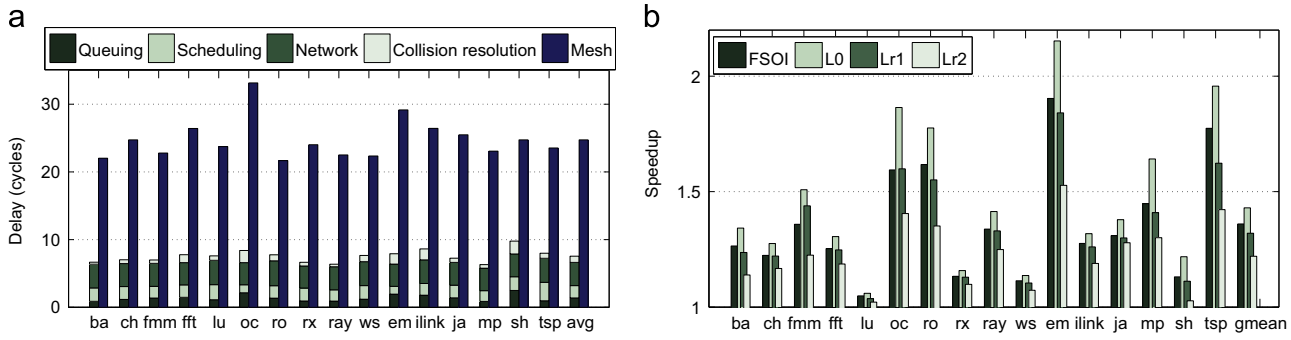

Fig. 10. Performance of 16-node systems with respect to different SPLASH-2 benchmark applications. (a) Total packet latency in the free-space optical interconnect (left) composed of four elements (queuing delay, scheduling delay, network latency, and collision resolution delay) and the conventional mesh (right). (b) Improvement in speed of free-space optical interconnect (FSOI) and several configurations of a conventional mesh relative to the baseline [20].

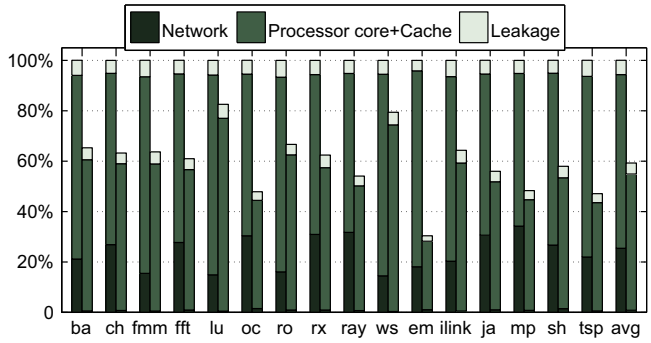

Fig. 11. Energy usage relative to the baseline mesh interconnect [20].

speedup as compared to the ideal 1.43. The FSOI also outperforms the aggressive L_{r1} (1.32) and L_{r2} (1.22) configurations.

In summary, the proposed interconnect offers an ultra-low communication latency and maintains a low latency as the system scales. The system significantly outperforms configured packet-switched interconnect. In addition, the performance gap is wider for larger scale systems and for those applications whose performance is more highly dependent on the interconnect.

5.3. Energy consumption analysis

A preliminary analysis of the energy characteristics of the proposed interconnect has also been examined. The total energy consumption of the 16-node system normalized to the baseline mesh configuration is shown in Fig. 11. Direct communication between nodes (cores) avoids the inherent inefficiency present in repeated buffering and processing in a packet-switched network. Additional energy savings is achieved through powering down the integrated VCSELs that are not in use, leading to an average power consumption of 1.8 W in the optical interconnect subsystem. The overall energy consumption in the interconnect is 20 × smaller than a mesh-based system. The faster execution also reduces the energy overhead elsewhere in the system. On average, the FSOI system achieves a 40.6% savings in energy. The reduction in energy savings is greater than the reduction in execution time, resulting in a 22% reduction in average power: 156 W for the system implementing a conventional interconnect and 121 W for the novel FSOI based system. The energy-delay product of the FSOI is 2.7 × (geometric mean) better than the baseline for the 16-node system.

5.4. Stressing the FSOI with extra data

The amount and pattern of traffic are determined by the behavior of the executing application. Although a diverse set of parallel applications are used, practical limitations exist to a brute force approach of expanding the number and types of applications. Synthetic traffic is also introduced in parallel to the program induced traffic to stress test the system against typical program behavior. The synthetic traffic is generated by forging read or write requests to legal addresses not currently in the L1 cache. Although some forged requests effectively become prefetches by chance, these requests are an insignificant minority. Application execution speedups obtained under 1 × and 2 × traffic loads are shown in Fig. 12. For every packet generated by the program, one or two more packets are generated to stress both the optical and mesh interconnects.

As shown in Fig. 12, the proposed FSOI based system does not exhibit added performance degradation due to collisions under a much exaggerated traffic load even without coordination or flow control. The degradation is consistent with traffic induced

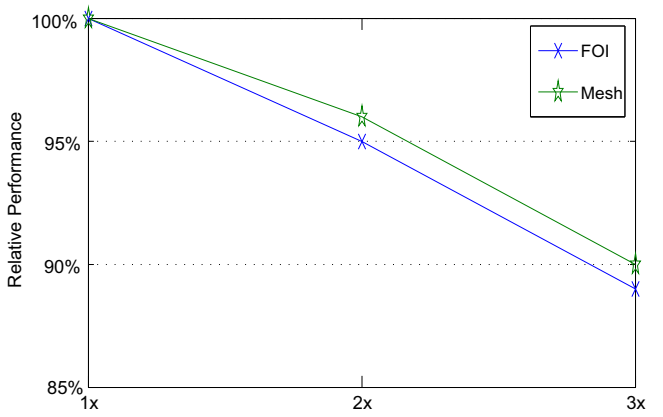

Fig. 12. Relative performance with extra traffic in both the optical and mesh interconnects [20].

serialization experienced by any interconnect, indicating strong robustness of the communication network under high loads.

6. Conclusions

A fundamental application of 3-D ICs is the integration of disparate technologies into a single stacked system. A 3-D integrated free-space optical interconnect system is described that merges CMOS technology with free-space optical interconnect. The system utilizes an all-to-all direct link network, where two cores are optically linked for core-to-core signaling. The FSOI also eliminates the constraints of the silicon optical modulators and switches, thereby increasing the bandwidth while reducing the total power consumed by a link.

Vertical cavity surface emitting lasers fabricated by the research group as well as commercial VCSELs included in the prototype experimentally verify the functionality of the 3-D integrated optical components. The photodetectors exhibit an operational bandwidth of 9.3 GHz.

The CMOS logic planes containing the transmitter and receiver for the FSOI and the microprocessor core are also discussed. The maximum bandwidth of the FSOI transmitter and receiver circuits is 10 GHz. A microprocessor operating at 333 MHz and the interface circuits required to transmit signals through the FSOI are described. A 64 bit data word is sent from the microprocessor transmitter to the serializer of the FSOI transmitter, which is sent via optical link through modulated light waves at an 850 nm wavelength produced by a VCSEL. On the receiving core, a photodetector converts the optical signal back into an electrical signal which is amplified and filtered before deserialization and storage in SRAM memory for the core to read.

3-D integrated circuit technology is the next generation in chip stacking processes. One of the most critical attributes of 3-D ICs is the ability of these systems to integrate disparate technologies. This defining attribute of 3-D ICs offers unique opportunities for highly heterogeneous and multi-functional systems such as the integrated CMOS and free-space optical interconnect system described in this work.

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